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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/738,649	12/15/2000	Charles P. Roth	10559/277001/P9284-ADI	1526

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EXAMINER	
HARKNESS, CHARLES A	

ART UNIT	PAPER NUMBER
2183	7

DATE MAILED: 10/22/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/738,649	ROTH ET AL	
	Examin r	Art Unit	
	Charles A Harkness	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 December 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 April 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Papers Submitted

1. It is hereby acknowledged that the following papers have been received and placed of record in the file: Drawings as received on 04/30/01; Change of Address as received on 12/06/02; and Information Disclosure Statement as received on 08/06/03.

Specification

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

3. The applicant or their representatives are urged to review the specification and submit corrections for all mistakes of a grammatical, clerical, or typographical nature.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-13, 15-19, 21-25, and 27 are rejected under 35 U.S.C. 102(b) as being anticipated by Alpert et al, U.S. Patent Number 5,740,413 (herein referred to as Alpert).

5. Referring to claim 1 Alpert has taught a method comprising:

selecting one of a plurality of debugging modes as a function of a current operating mode of a processor (Alpert column 4 line 62-column 5 line 5, column 5 line 59-column 6 line 19).

6. Referring to claim 2 Alpert has taught further comprising raising an exception after executing an instruction (Alpert column 1 lines 42-65; if there is a handler for an exception, than an exception must occur, column 14 lines 5-27).

7. Referring to claim 3 Alpert has taught further comprising invoking an emulation mode of the processor after executing an instruction (Alpert column 2 lines 52-57).

8. Referring to claim 4 Alpert has taught wherein selecting the debugging mode comprises selecting a first debugging mode when the operating mode comprises user mode, and selecting a second debugging mode when the operating mode comprises supervisor mode (Alpert column 4 lines 17-32, column 5 line 59-column 6 line 19, column 8 lines 51-55).

9. Referring to claim 5 Alpert has taught a method comprising:

receiving an instruction (Alpert figures 2, 3 and 5);

receiving a signal;

selecting a mode of debugging as a function of the signal, wherein selecting the debugging mode comprises selecting a first de bugging mode when the signal is a first signal, and selecting a second debugging mode when the signal is a second signal (column 8 lines 51-55; since the system has different debug events for different modes, some signal must be present to show the system which mode it is in); and

executing the instruction (Alpert figures 2, 3 and 5).

10. Referring to claim 6 Alpert has taught further comprising raising an exception (Alpert column 1 lines 42-65; if there is a handler for an exception, than an exception must occur, column 14 lines 5-27).

11. Referring to claim 7 Alpert has taught further comprising invoking an emulation event (Alpert column 2 lines 52-57).

12. Referring to claim 8 Alpert has taught further comprising:

sensing register contents (Alpert column 6 lines 12-19, column 8 lines 10-28 and 37-41, column 7 lines 27-52); and

outputting register contents (Alpert column 6 lines 12-19, column 8 lines 10-28 and 37-41, column 7 lines 27-52).

13. Referring to claim 9 Alpert has taught wherein the instruction is received by a processor adapted to operate in a plurality of states, the method further comprising:

sensing states of the processor (Alpert column 6 lines 12-19, column 8 lines 10-28 and 37-41); and

outputting states of the processor (Alpert column 6 lines 12-19, column 8 lines 10-28 and 37-41).

14. Referring to claim 10 Alpert has taught wherein the instruction is received by a processor, the method further comprising selecting a mode of single-step debugging as a function of the operating mode of the processor (Alpert column 1 lines 63- column 12 line 27).

15. Referring to claim 11 Alpert has taught a device comprising:

a processor, the processor adapted to operate in a plurality of operating modes including an emulation mode (Alpert column 2 lines 52-57);

a control register adapted to store the state of a control bit (Alpert column 6 lines 12-19); and

an exception handler (Alpert column 1 lines 42-65);

wherein the processor is adapted to select one of a plurality of debugging modes as a function of the control bit (Alpert column 8 lines 51-55, column 7 lines 44-52).

16. Referring to claim 12 Alpert has taught wherein the processor is adapted to select one of a plurality of debugging modes as a function of the current operating mode of the processor (Alpert column 8 lines 51-55).

17. Referring to claim 13 Alpert has taught further comprising exception logic adapted to sense the state of the control bit and to trigger an exception event as a function of the state of the control bit (Alpert column 14 lines 35-56).

18. Referring to claim 15 Alpert has taught wherein the control bit is a first control bit, the system further comprising a second control bit, and wherein the mode of single-step debugging is a function of the state of the second control bit (Alpert column 6 lines 17-37, column 7 lines 44-52).

19. Referring to claim 16 Alpert has taught wherein the processor is a digital signal processor (Alpert abstract, backround; Alpert uses digital signals to execute all functions in the system described).

20. Referring to claim 17 Alpert has taught a device comprising:

a processor, the processor adapted to operate in a plurality of operating modes ;

wherein the processor is adapted to select one of a plurality of debugging modes as a function of the current operating mode of the processor (Alpert column 4 lines 17-32, column 5 line 59-column 6 line 37, column 8 lines 51-55, column 7 lines 44-52).

21. Referring to claim 18 Alpert has taught further comprising a control register adapted to store the state of a control bit (Alpert column 4 lines 17-32, column 5 line 59-column 6 line 37, column 8 lines 51-55, column 7 lines 44-52),

wherein the processor is adapted to select one of the plurality of debugging modes as a function of the state of the control bit (Alpert column 4 lines 17-32, column 5 line 59-column 6 line 37, column 8 lines 51-55, column 7 lines 44-52).

22. Referring to claim 19 Alpert has taught further comprising:

an exception handler (Alpert column 1 lines 42-65); and

logic adapted to sense the state of the control bit and to trigger an exception event as a function of the state of the control bit (Alpert column 14 lines 35-56).

23. Referring to claim 21 Alpert has taught wherein the processor is a digital signal processor (Alpert abstract, backround; Alpert uses digital signals to execute all functions in the system described).

24. Referring to claim 22 Alpert has taught a system comprising:

a processor, the processor adapted to operate in a plurality of operating modes (Alpert column 4 lines 17-32, column 5 line 59-column 6 line 19, column 8 lines 51-55);

a control register adapted to store the state of a control bit (Alpert column 4 lines 17-32, column 5 line 59-column 6 line 19, column 8 lines 51-55);

an input/output device (Alpert figure1 keyboard and display); and

an exception handler (Alpert column 1 lines 42-65);

wherein the processor is to adapted to select one of a plurality of debugging modes as a function of the control bit (Alpert column 4 lines 17-32, column 5 line 59-column 6 line 37, column 8 lines 51-55, column 7 lines 44-52).

25. Referring to claim 23 Alpert has taught wherein the processor is adapted to select one of a plurality of debugging modes based upon the current operating mode (Alpert column 8 lines 51-55).

26. Referring to claim 24 Alpert has taught further comprising a memory device coupled to the processor (Alpert column 5 lines 21-23).

27. Referring to claim 25 Alpert has taught further comprising logic adapted to sense the state of the control bit and to trigger an exception event as a function of the state of the control bit (Alpert column 1 lines 42-65, column 14 lines 35-56).

28. Referring to claim 27 Alpert has taught wherein the control bit is a first control bit, the system further comprising a second control bit, wherein the processor is adapted to select one of a plurality of debugging modes based upon the state of the second control bit (Alpert column 6 lines 17-37, column 7 lines 44-52).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

29. Claims 14, 20, and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Edgington et al, U.S. Patent Number 5,530,804 (herein referred to as Edgington).

30. Referring to claims 14, 20, and 26 Alpert has not explicitly taught further comprising logic adapted to sense the state of the control bit and to trigger an emulation event as a function of the state of the control bit. Edgington has taught further comprising logic adapted to sense the state of the control bit and to trigger an emulation event as a function of the state of the control bit (Edgington abstract). It would have been obvious to one of ordinary skill in the art at the time of the invention to have an emulation mode. By emulating, a system can debug software to find mistakes and errors in the code. By fixing the errors, the programmer can get the results they desire. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to have an emulation mode to allow the programmer to find the errors in the code and have a program that works correctly.

Conclusion

31. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure as follows. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR 1.111(c).

Borkenhagen et al., U.S. Patent Number 5,790,843 has taught using a debuging systerm.

Efficient Mechanism for Multiple Debug Modes", IBM Technical Disclosure Bulletin, has taught using different types of debugging modes.

32. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Charles A Harkness whose telephone number is 703-305-7579. The examiner can normally be reached on 8:00 A.M. – 5:30 P.M. with every other Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on 703-305-9712. The fax phone numbers for the

organization where this application or proceeding is assigned are 703-746-7239 for regular communications and 703-746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-7579.

Charles Allen Harkness

Patent Examiner

Art Unit 2183

October 18, 2003